Preventing Potential-Induced Degradation in Crystalline Silicon PV Modules: Relationship Between Degradation and Bill of Material

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Outlook

1. Potential-Induced Degradation (PID): a sneaky problem;

2. Preventing PID at module level:

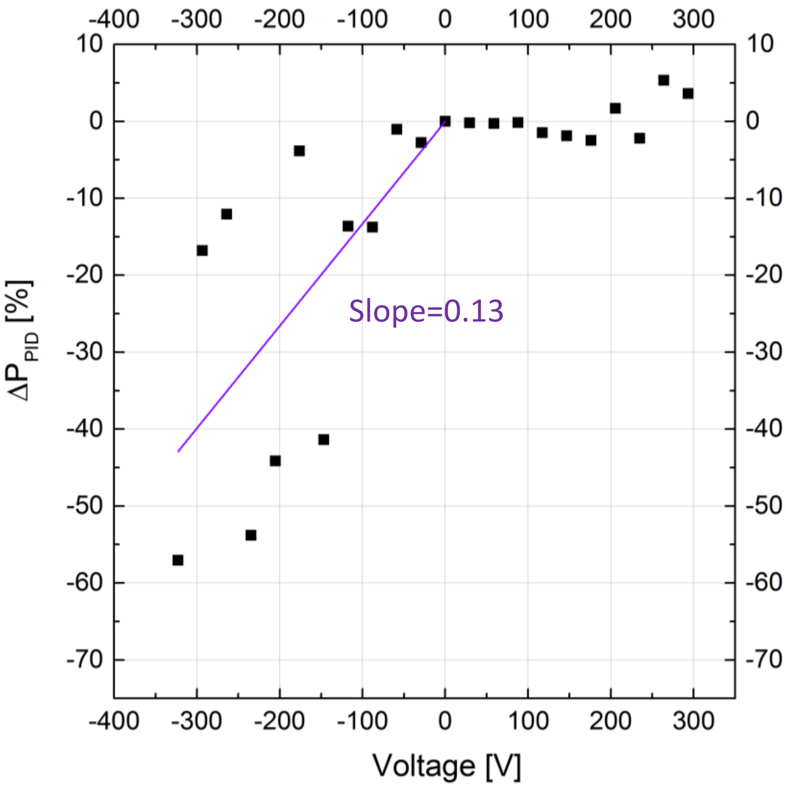
   relationship between PID and Bill-of-Material (BOM), (with focus on p-type c-Si cells/modules).

«*One-type* fits all» modules (independent of inverter choice and system configuration) carry a considerable commercial advantage.

3. Conclusions & …some reflections.

PID: a sneaky problem (1)

1. PID is not acting uniformly on modules in a string.



Greece,
~6 MW_p plant
Mono c-Si modules,
floating ground.

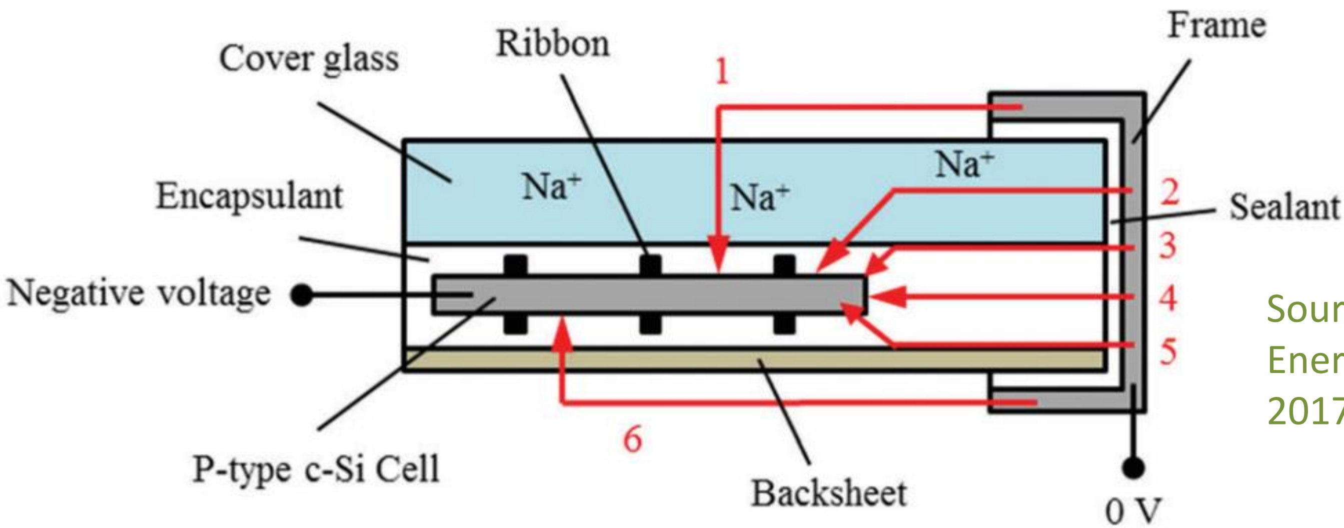
String loss ~ -14%

PID: a sneaky problem (2)

2. PID depends on a **combination of causes**:

- **Climatic conditions** of installation site;
- Other **location-specific conditions**: salt-mist (coastal areas) or soiling could promote PID;
- **System design**: grounding, inverter choice, etc. ;
- **Module design:**
  - mounting solutions: frame vs rail bars;
  - **bill of material** (BOM) used in sandwich manufacturing

Leakage currents pathways in c-Si modules



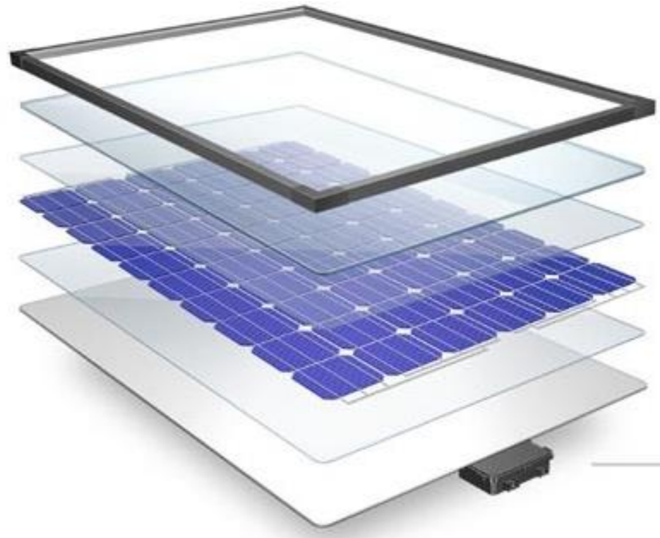
Source: Wei Luo et al., Energy Environ. Sci., 2017,10,43

Pathway 1 is the most detrimental: drift of Na^+ ions from glass when cells are at negative voltage.

Pathway 1 requires a conductive layer on top of glass: dew, rain, condensation, conductive soiling, ….

c-Si solar modules and BOM

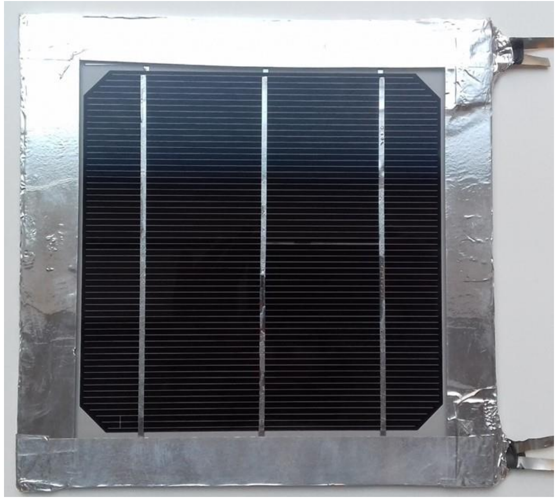
Due to constant downward cost pressure, we focus on <u>cost-effective solutions</u> only:



- ~~**Glass**~~
- **Cells**: std p-type (Al BSF) vs PID-free cells;
- **Encapsulants**: **EVA** high vs low volume resistivity ρ;
- **Backsheet (BS):** high vs low permeability (Water Vapor Transmission Rate WVTR).

Test samples: 1-cell mini-modules

Material		
Cells	Standard c-Si (**std-cell**)	PID-free cell (**PID-free**)
Encapsulants **EVA**	EVA high resistivity (**EVA-high-ρ**) $\rho > 1{\cdot}10^{15}\ \Omega{\cdot}\mathrm{cm}$	EVA low resistivity (**EVA-low-ρ**) $\rho > 6{\cdot}10^{14}\ \Omega{\cdot}\mathrm{cm}$
Backsheets **PVF/PET/PVF**	BS high permeability (**BS-high-P**) Thickness: 0.17 mm WVTR ~ 1.8 $g/m^2/d$	BS low permeability (**BS-low-P**) Thickness: 0.35 mm WVTR ~ 0.7 $g/m^2/d$



Al tape simulating frame

$2^3 = 8$ combinations of samples

PID testing

1. IEC TS 62804-1:2016

Photovoltaic (PV) modules – Test methods for the detection of potential-induced degradation – Part 1: Crystalline silicon

Two types of test:

- *Climatic chamber*: ***60°C, 85%-RH (60/85), 96 h, ±1000 V***;

  higher stresses possible: ***85°C, 85%-RH (85/85)***;

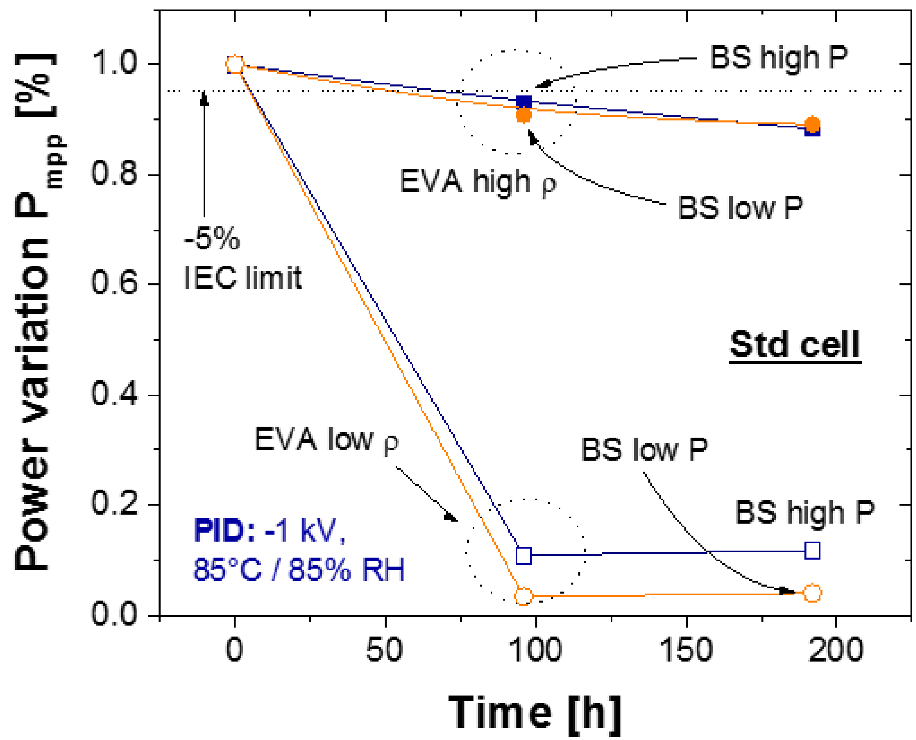
- *Dry test (Al foil): 25°C, <60% RH, 168 h, ±1000 V;*

"The stress-test levels in this Technical Specification have not been related to those of the natural environment.

Modules types undergoing damp heat chamber testing with a 60 °C and 85 % relative humidity stress level for 96 h were found resistant to PID in outdoor tests in Florida."

Standard cells (85/85)

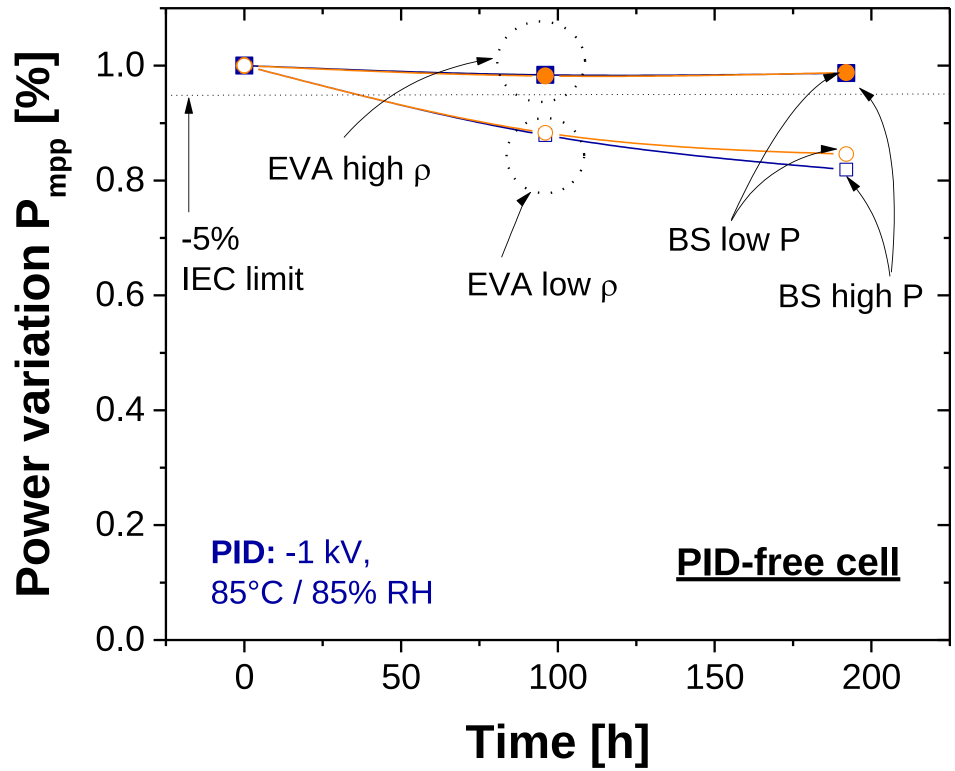
Std cells: 1-cell mini-modules tested at **85°C/85% RH/-1000 V**



1. Huge difference between high/low resistivity encapsulant;
2. Effect from backsheet is negligible.

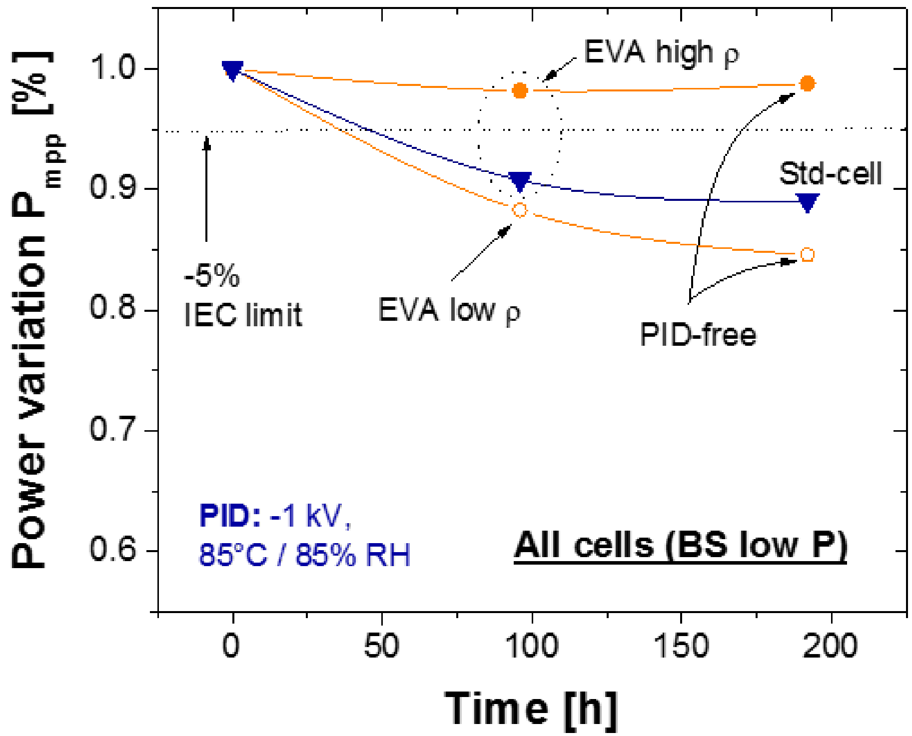
PID-free cells (85/85)

PID-free cells: 1-cell mini-modules tested at **85°C/85% RH/-1000 V**



1. Difference between high/low resistivity encapsulant;
2. Effect from backsheet is negligible.

All cells, low-permeability backsheet (85/85)



All cells,
1-cell mini-modules tested at
85°C/85% RH/-1000 V

Best material combinations

	"PID-free" cell	Standard cell
EVA high ρ	1	2
EVA low ρ	3	4

PID-free cells suffer less, but:
std-cell with high-ρ EVA experiences less degradation than PID-free cell with low-ρ EVA.

PID testing, power loss (%): 85/85 vs 60/85

85°C/85% RH/-1000 V

Cells	EVA	BS high P (96 / 192 h) [%]	BS low P (96 / 192 h) [%]
STD c-Si cells	High ρ	-6.9 / -11.7	-9.2 / -10.9
	Low ρ	-89.1 / -88.2	-96.6 / -96
PID-free c-Si cells	High ρ	-1.6 / -1.3	-1.8 /-1.2
	Low ρ	-12.1 / -18.1	-11.7 / -15.4

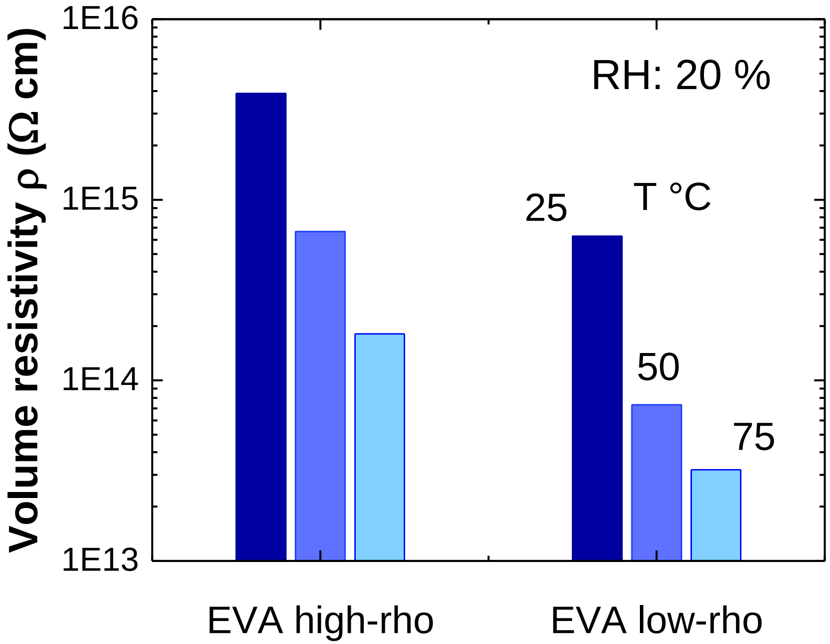
60°C/85% RH/-1000 V

Cells	EVA	BS high P (96 / 192 h) [%]	BS low P (96 / 192 h) [%]
STD c-Si cells	High ρ	-0.7 / -0.1	-0.8 / -0.4
	Low ρ	-85 / -83.5	-77.9 / -76
PID-free c-Si cells	High ρ	-0.2 / 0	-0.3 / -0.1
	Low ρ	-0.7 / -1	-1.7 / -1

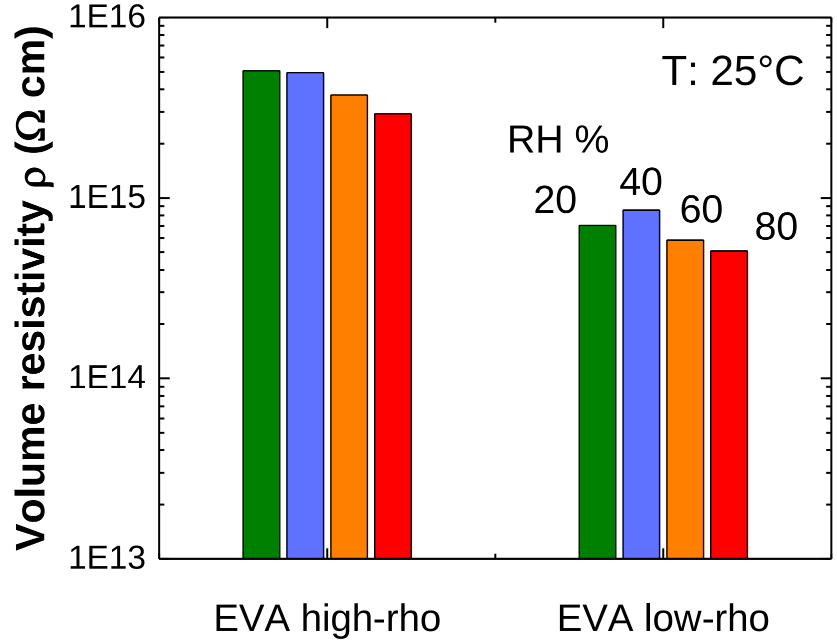
60/85: only combination suffering PID are **std cells with low-ρ EVA.**
No effect of **backsheet.**

Resistivity (ρ) measurements on EVA encapsulants

ρ (T), RH = 20%



ρ (RH), T = 25 ° C



IEC 62788-1-2 standard (method B)

- Slight effect of **relative humidity** (RH) on ρ

  >>> can partly explain why effect of backsheet is not relevant;

- Considerable effect of **temperature** (T) on ρ

  >>> explains why 85/85 conditions are much harsher than 60/85

Conclusions (1)

Testing at 85°C/85%-RH, conclusions:

- Strong effect of **EVA** (low vs high ρ) on **<u>all cells</u>**;
- **Cells:** PID-free cells work better, but: std-cell with high-ρ EVA experiences less degradation than PID-free cell with low-ρ EVA;
- No effect from **back-sheet**;
- If we stick to the IEC -5% threshold (96 hrs): only combination passing test is **PID-free cell with high-ρ EVA;**

Testing at 60°C/85%-RH, conclusions:

- Strong effect of **EVA** (low vs high ρ) on **<u>conventional cells only;</u>**
- No effect from **back-sheet**;

Conclusions (2)

- Our results: 1-cell mini-modules.

  >>> How results translate to large-area (60 – 72-cell) modules?

- 1-cell mini-modules constitute a sort of worst-case "situation", as "edge-effects" are more pronounced.

- It is possibly not meaningful to stick to IEC -5% threshold, or power loss values (%) in absolute terms, but results are consistent/reproducible and give clear indications on how to optimize the selection of materials to prevent PID at the module level.

The end of PID ?

Problem is «well/partly» understood for p-type c-Si cells/modules, and solutions exist, but:

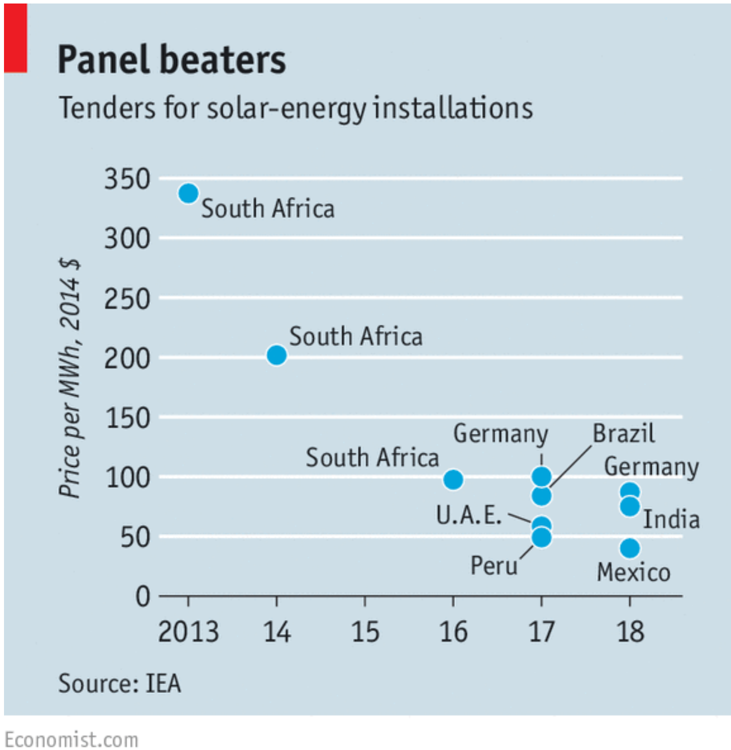
1. New technologies for which PID degradation mechanisms are less understood :

   n-type, PERC, IBC, SHJ, passivated-contacts, thin films, etc.;

2. Clear trend to move to higher string voltages (1500 V, 2000 V?);

3. Global market characterized by dramatic cost-reduction dynamics;

Announced long-term contract prices for solar projects



Source: Economist, April 2016 &
IEA: Müller et al. EUPVSEC 2016

- Auction results point to a wave of **very low cost projects** coming on-line over coming years;
- Global market dominated by large players;
- Dramatic **cost-reduction dynamics** to win bids and sign PPA's (Power Purchase Agreements)
- IPP's (Indipendent Power Producers) to **squeeze margins** all along the value chain: EPC's (Engineering, Procurement, Commisioning contractors), suppliers of components (modules, inverters, BOS, etc.), …

Thank you for your attention!

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