Origin of PID-s

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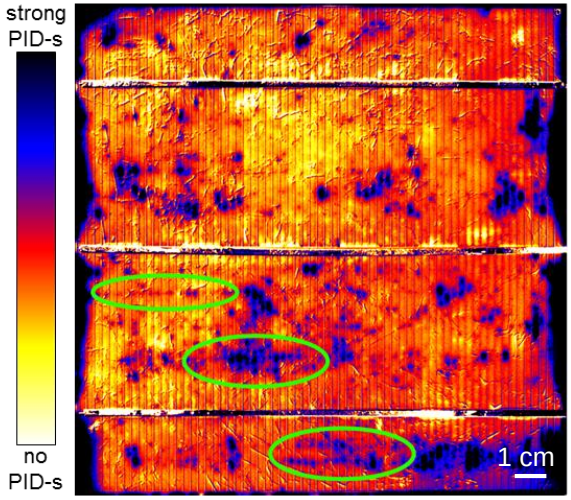

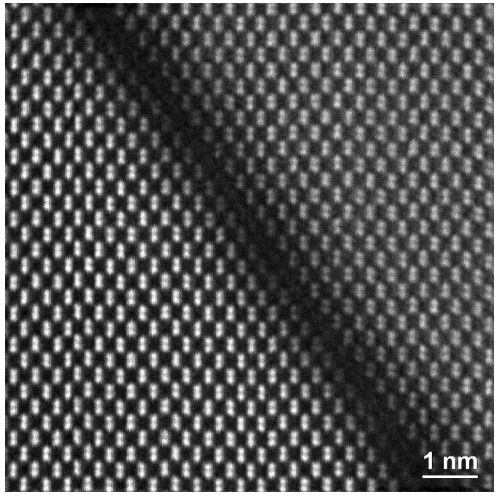

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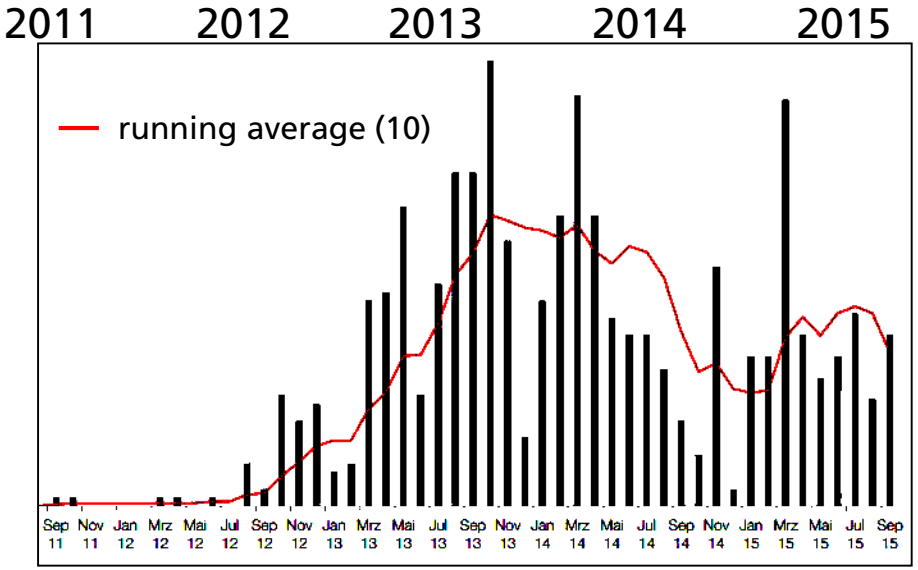
Background
PID is still in the field

- Potential induced degradation (PID) of solar modules leads to yield losses
- Counter-measures against PID known since a few years, **but costly**
- PID ‘of the shunting type’ of c-Si PV modules (PID-s) is an ongoing issue!

PV power plants with confirmed cases of PID in Europe [1]



Frequency of new complaints in Europe by month [2]

[1] C. Hinz et al., PADCON PID Workshop, 10.11.2015, http://padcon.de/content/site/dateien/2620Vergleich_von_unterschiedlichen_Regenerationsmethoden_fuer_PID.pdf
[2] Benjamin Sandrock et al., PADCON PID Workshop, 08.04.2016. http://padcon.de/content/site/dateien/2733Suncycle_PID____Sicher_erkennen_und_erfolgreich_heilen.pdf

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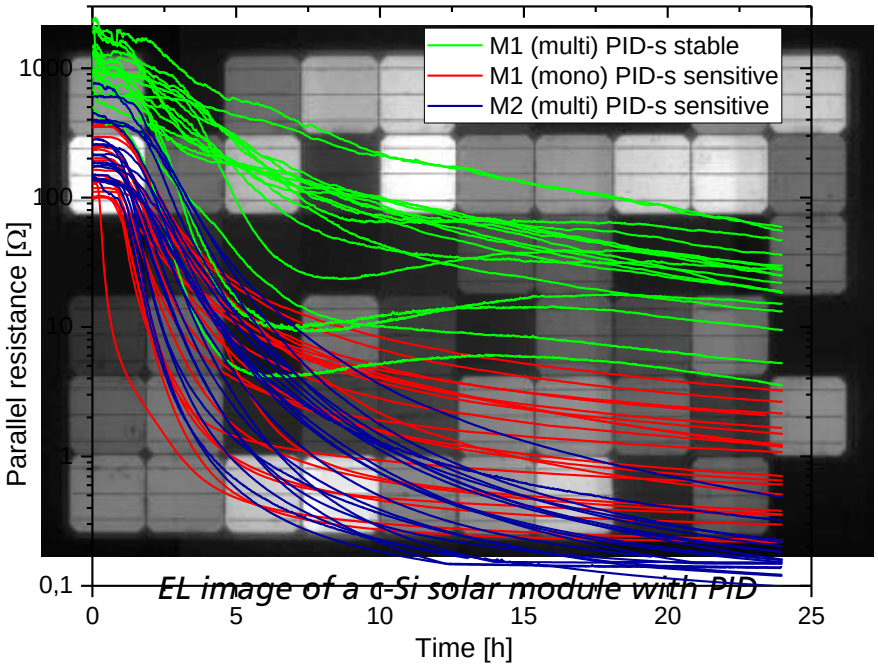
Motivation
Variation of PID-s susceptibility

- Variation of PID-shunting (PID-s) sensitivity of individual cells:
  - On module level: “checkerboard pattern”
  - On cell level: fluctuation of $R_{shunt}(t)$ of ‘similar’ cells

‘PIDcon’



EL image of a c-Si solar module with PID

→ Reason for variation?

→ Inherent stability against PID-s?

Aim of this talk:

- Initial defects of PID-shunts

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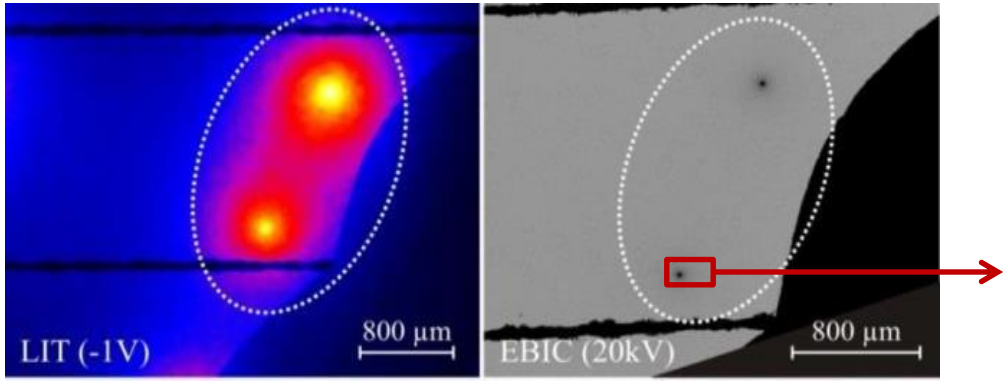
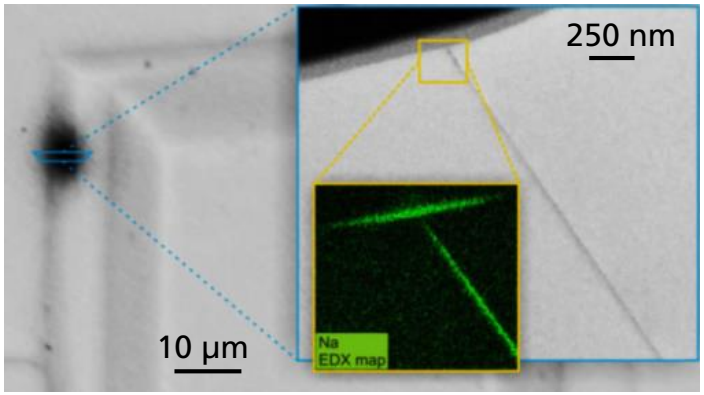
Outline

- PID-s root cause analysis
  - Type of stacking faults
- Quest for PID-s defect precursors
  1) Primordial stacking faults
  2) Threading dislocations
  3) Surface defects
- Conclusion

PID-s root cause analysis
Results in a nut-shell





- Local hot spots on degraded cells [1]
- PID-shunting ('PID-s') of p-n junction by Na-decorated stacking faults [2]*
- Out-diffusion of Na during recovery [3]
- Na-decoration even found after corona test [4]

[1] V. Naumann et al., Microstructural Analysis of Crystal Defects Leading to Potential-Induced Degradation (PID) of Si Solar Cells, Energy Procedia 33, 76 (2013).
[2] V. Naumann et al., Explanation of potential-induced degradation of the shunting type by Na decoration of stacking faults in Si solar cells, Sol. Energ. Mat. Sol. Cells 120, 383 (2014).
[3] D. Lausch et al., Sodium Outdiffusion from Stacking Faults as Root Cause for the Recovery Process of Potential-Induced Degradation (PID), Energy Procedia 55, 486-493 (2014).
[4] V. Naumann et al., Sodium decoration of PID-s crystal defects after corona induced degradation of bare silicon solar cells, Energy Procedia 77, 397-401 (2015).

* independently confirmed by: S. P. Harvey et al., Sodium Accumulation at Potential-Induced Degradation Shunted Areas in Polycrystalline Silicon Modules, IEEE Journal of Photovoltaics 99, 1-6 (2016).

PID-s root cause analysis

Current model for PID-s [1]

- High field strength causes drift of Na^+ through the SiN_x layer
- Na accumulates at SiN_x/Si interface and penetrates into stacking faults

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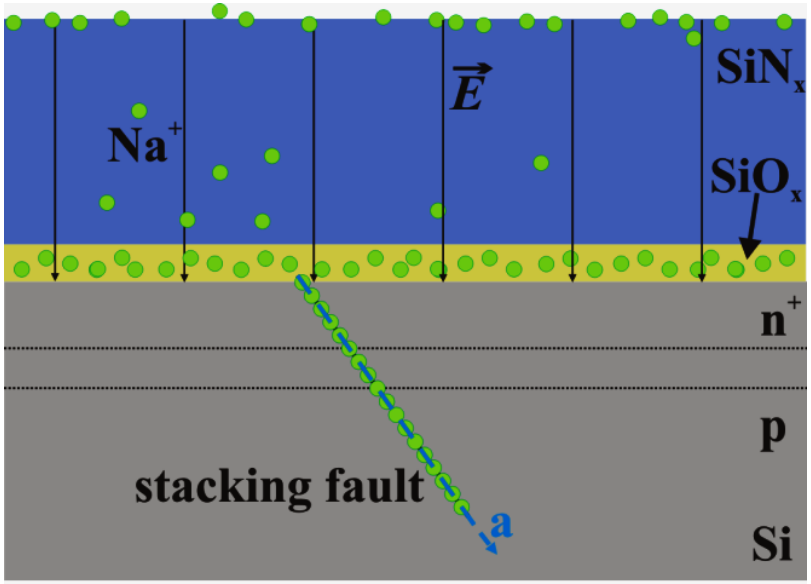
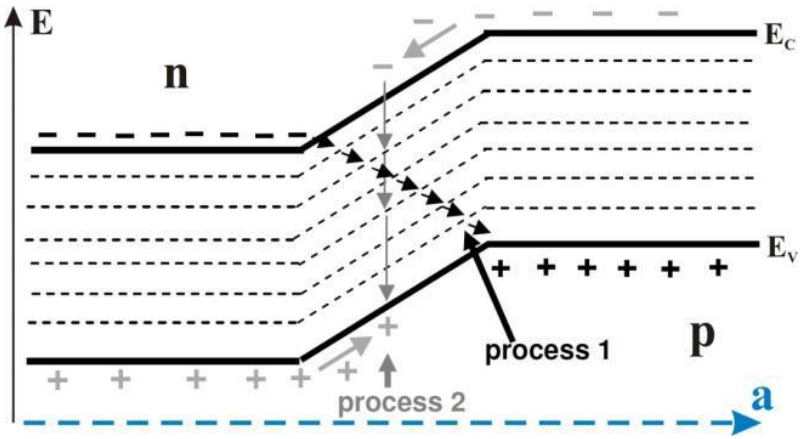
- Shunting of the p-n junction through defect levels of the highly decorated stacking fault (SF) → shunting, process 1
- Recombination process via defect states in depletion region → increased J_{02} and $n_2 > 2$, process 2
- "Most favorable configuration is a SF fully filled with Na atoms..." [2]

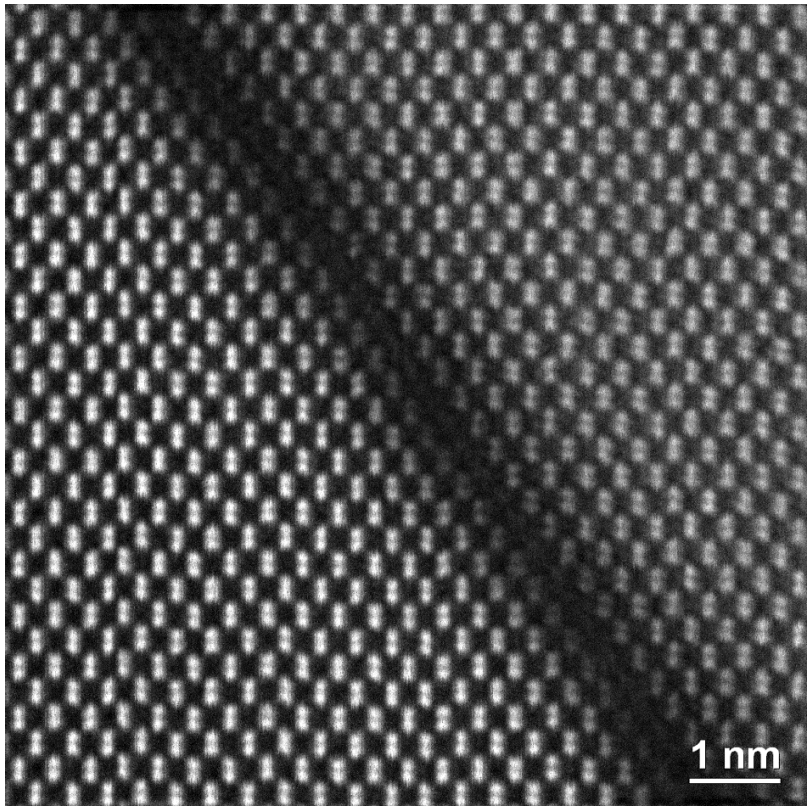




[1] V. Naumann et al., Solar Energy Materials and Solar Cells 120 (2014), 383-389.
[2] B. Ziebarth et a., PID in solar cells: Electronic structure and diffusion mechanism of sodium in stacking faults of silicon, Journal of Applied Physics 116, 093510 (2014)

PID-s root cause analysis

Scanning Transmission Electron Microscopy (STEM)

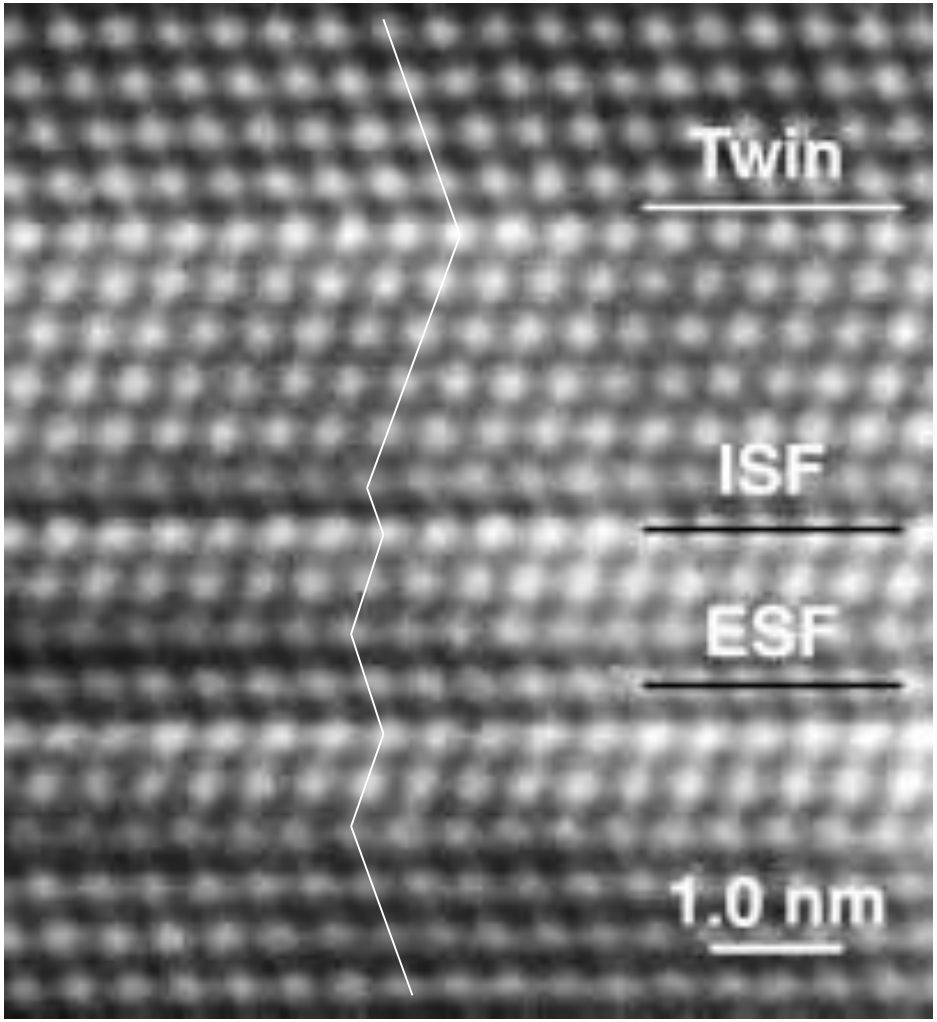


STEM image of a Na decorated planar defect in a {111}-plane

- STEM investigations verify "modified" stacking faults in {111}-planes [1]

[1] V. Naumann et al., Phys. Status Solidi RRL 7, No. 5, 315–318 (2013).

Type of stacking faults?
Intrinsic vs. extrinsic



Differentiation of stacking faults (SFs) by TEM:

- Intrinsic SF: single fault layer
- Extrinsic SF: double fault layer

TEM-micrograph of SFs and twin boundary in thin film silicon [NREL]
http://www.nrel.gov/docs/fy00osti/22211.pdf

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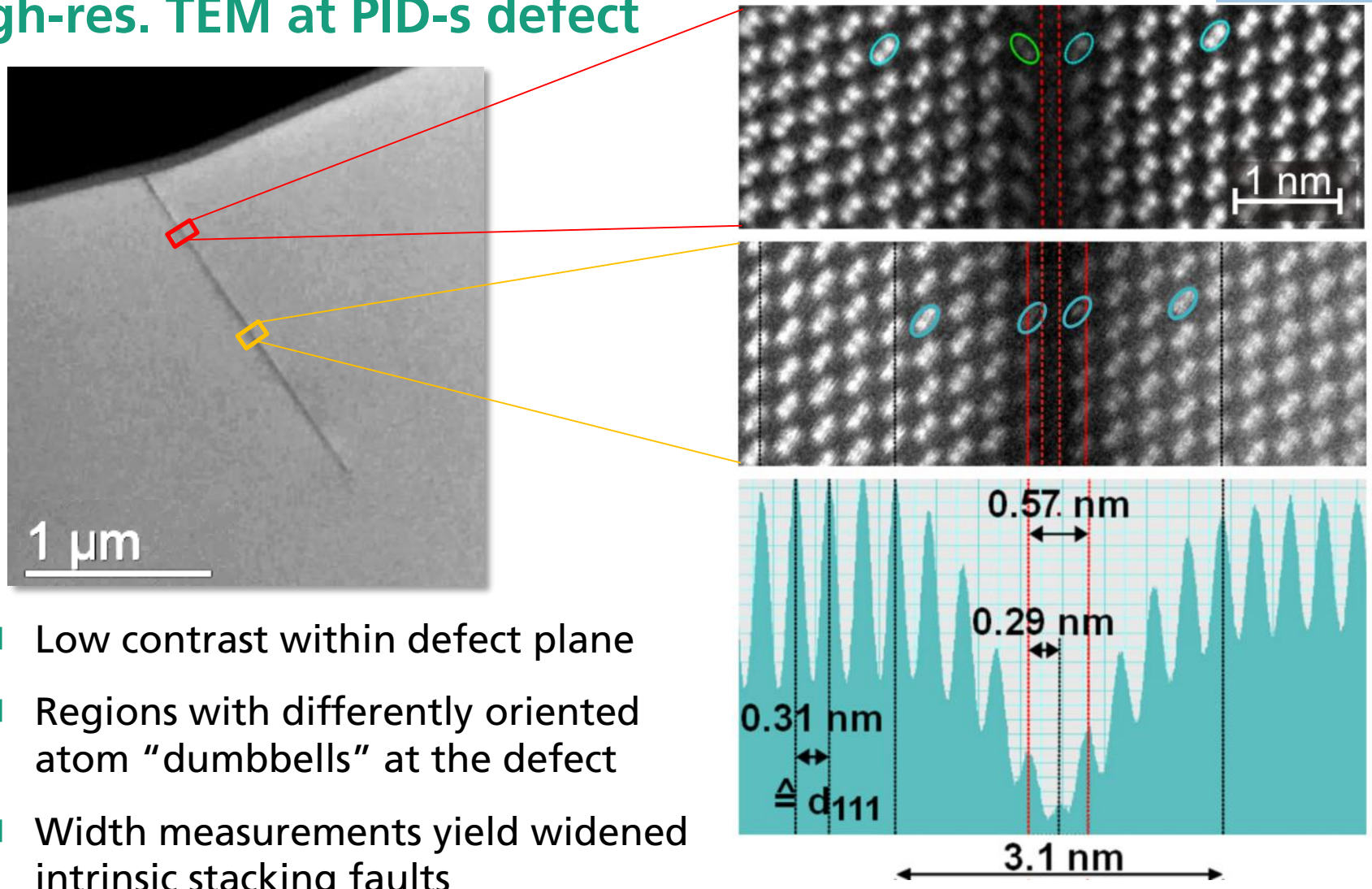
Type of stacking faults?
High-res. TEM at PID-s defect



- Low contrast within defect plane
- Regions with differently oriented atom "dumbbells" at the defect
- Width measurements yield widened intrinsic stacking faults

[1] V. Naumann et al., Solar Energy Materials & Solar Cells 120, 383 (2014).

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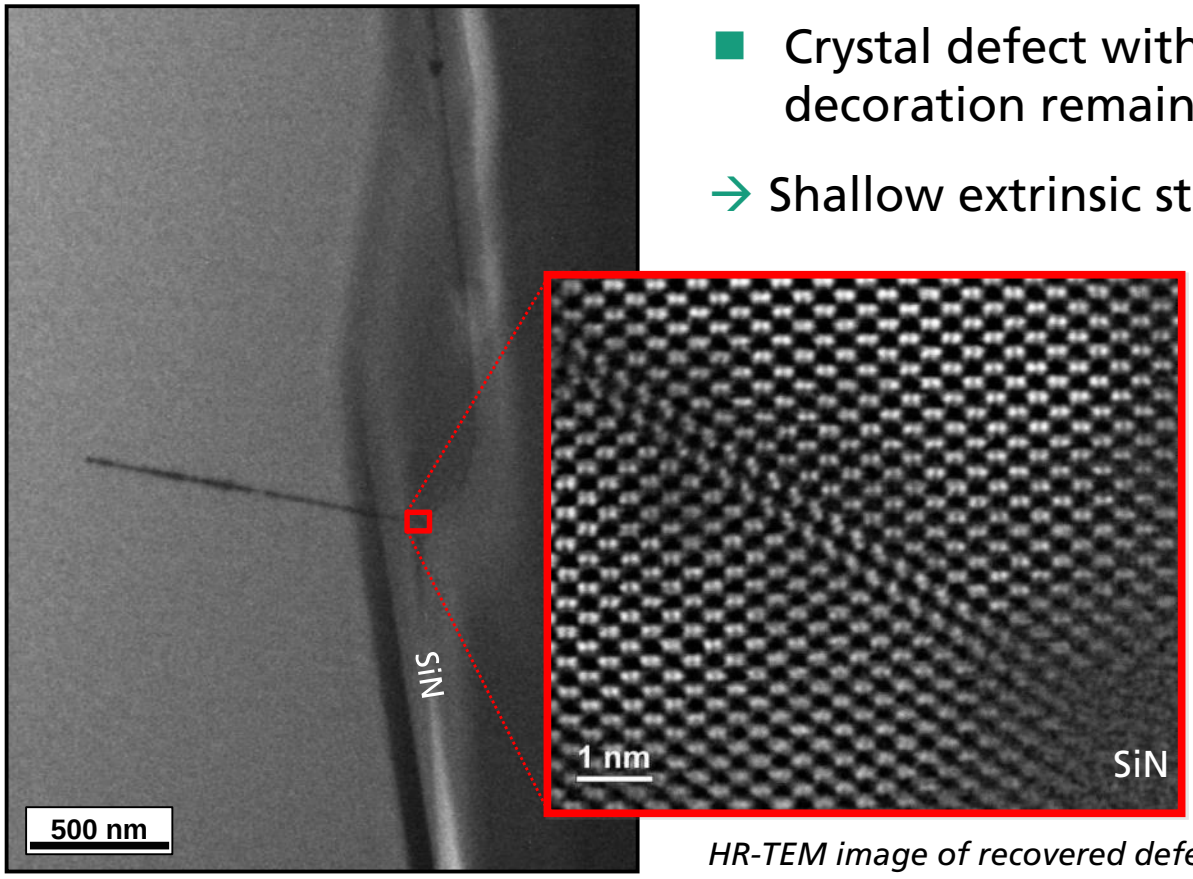
Type of stacking faults?
Partially recovered PID-s defect

- TEM image of an annealed PID-s defect



- Crystal defect without Na decoration remains in Si

→ Shallow extrinsic stacking fault

HR-TEM image of recovered defect near the SiN_x interface

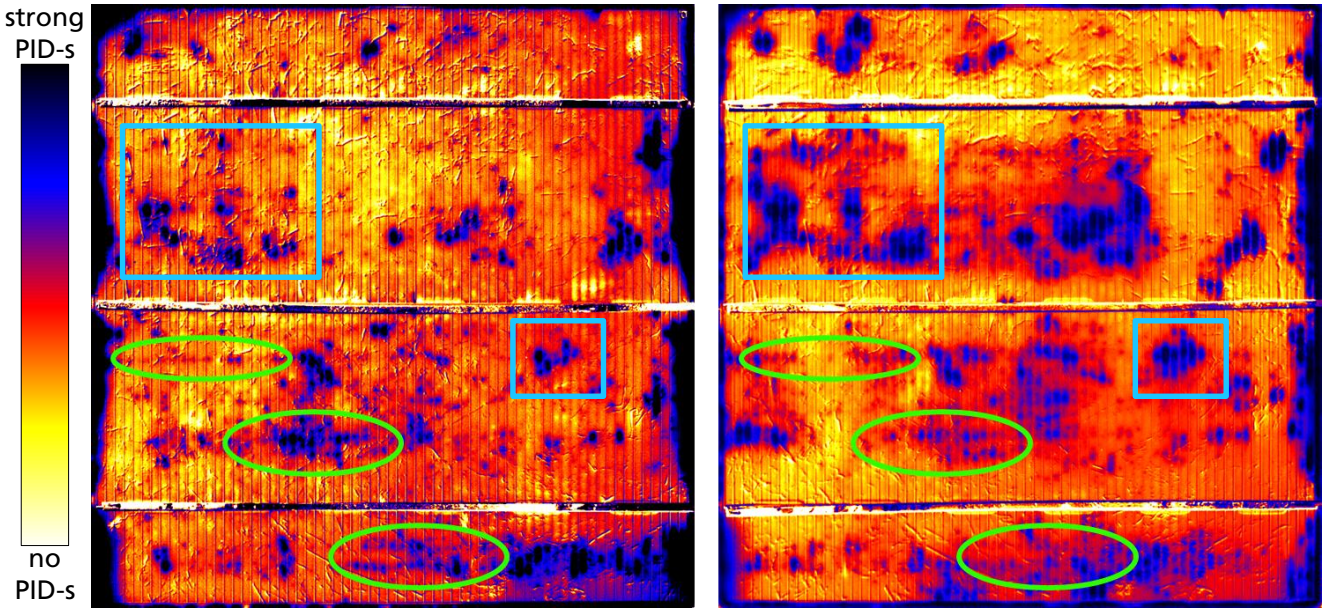
[1] V. Naumann, D. Lausch, A. Hähnel, O. Breitenstein, C. Hagendorf, Nanoscopic studies of 2D-extended defects in silicon that cause shunting of Si-solar cells, physica status solidi (c) 12 (8), 1103–1107 (2015).

Outline

- PID-s root cause analysis
  - Type of stacking faults
- Quest for PID-s defect precursors
  1) Primordial stacking faults
  2) Threading dislocations
  3) Surface defects
- Conclusion

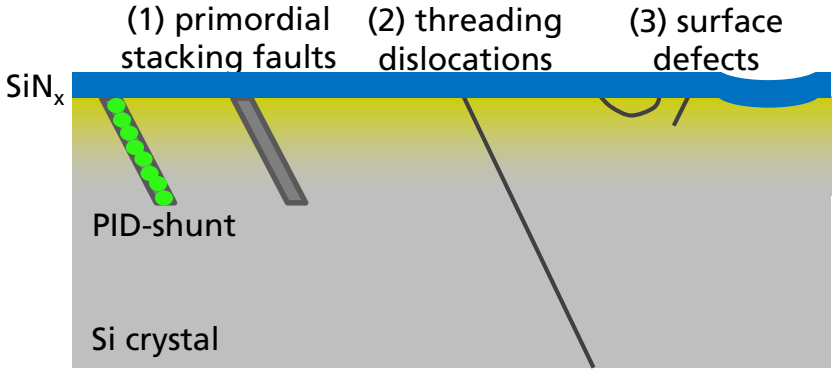
New hints: PID tests at neighboring cells

PID-shunt maps after equal PID tests:



„PID-shunt map“
= $EL_{PID\text{-}s}$ / $EL_{initial}$

- PID-shunts exist at same positions
- Indication of material and/or process related defect precursors:



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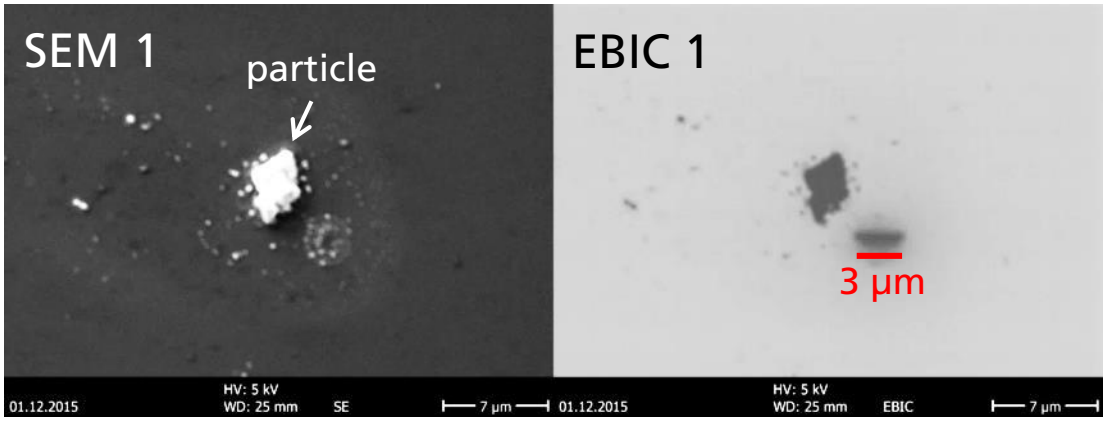
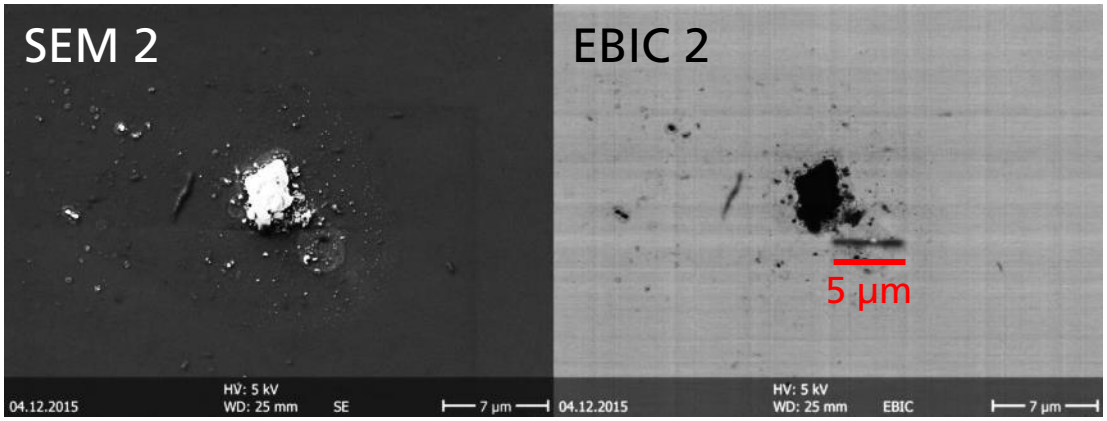
1) Primordial stacking faults?

Growth of PID-s defects during sequential PID stress

after 1st PID test



after 2nd PID test



PID 1
85 °C, 600 V, 2 hours

SEM/EBIC 1

PID 2
85 °C, 600 V, 24 hours

SEM/EBIC 2

- Defects grow in lateral extension under high voltage stress [1]
- Indicates that stacking faults do not exist before high voltage stress

[1] V. Naumann et al., Investigations on the formation of stacking fault-like PID-shunts, Energy Procedia 92, 569 - 575 (2016).

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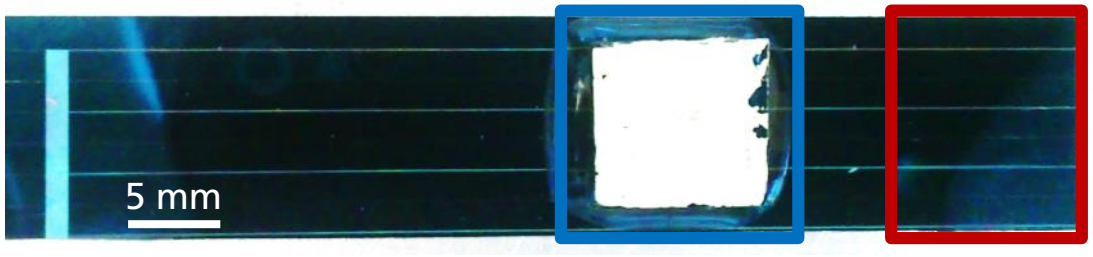
1) Primordial stacking faults?
Defect etch for delineation of stacking faults

- Cz p-type solar cell with polished front side and SiN_x
- PIDcon test on ~10x12 mm² using EVA/glass-stack (1000 V, 85 °C, 22 hours)
- Two samples:

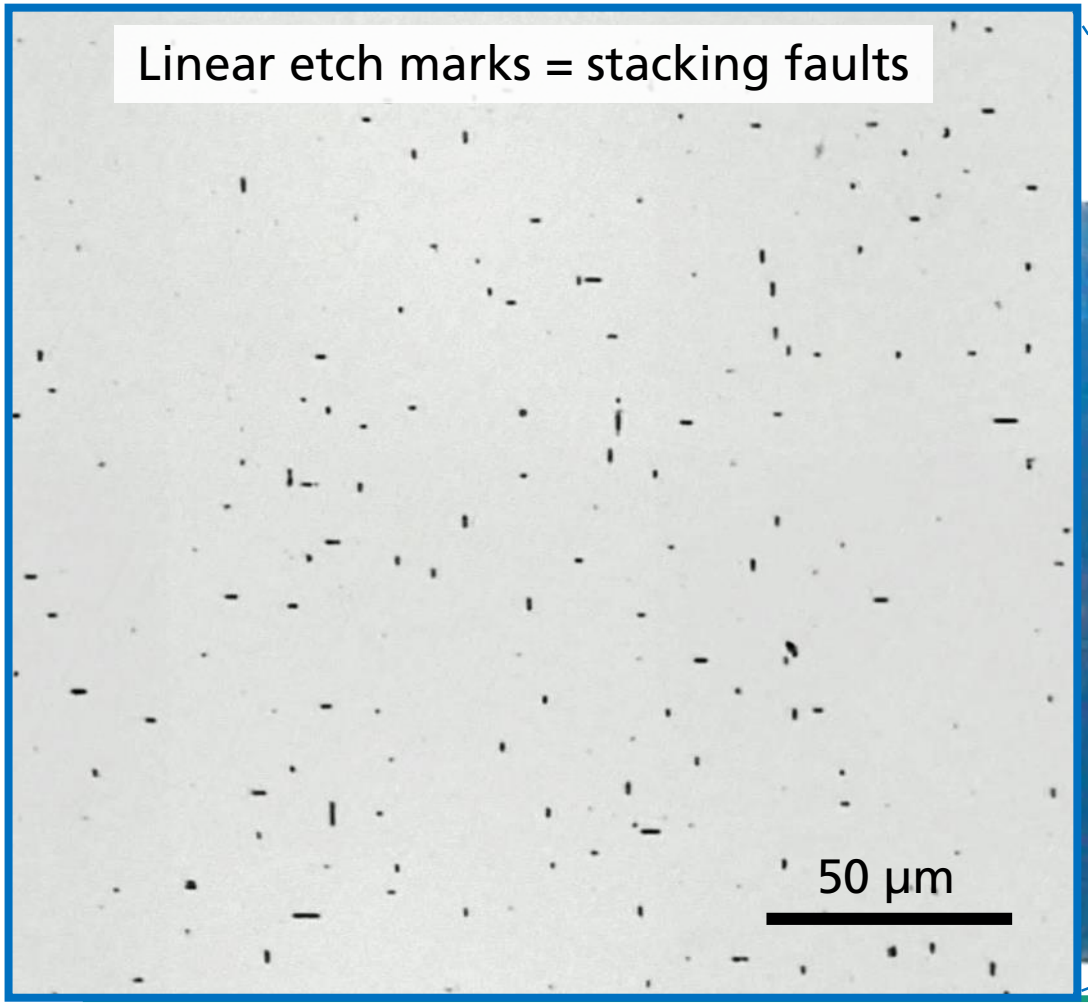


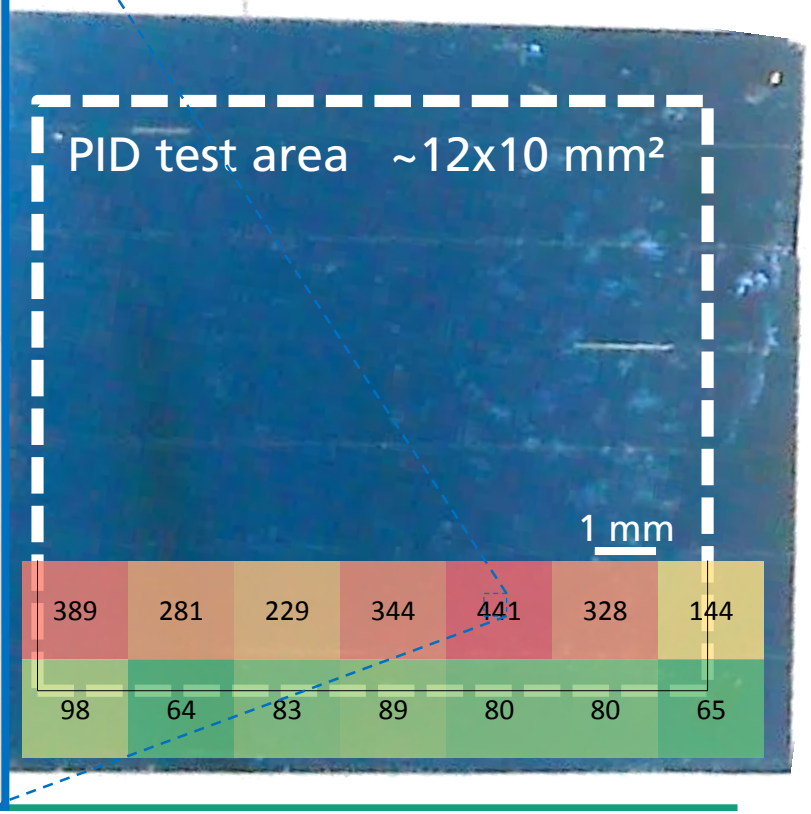
- SiN_x removal and subsequent defect etch → delineation of stacking faults
- Optical microscopy → image processing → count of linear features in sub-images

[1] V. Naumann et al., Investigations on the formation of stacking fault-like PID-shunts, Energy Procedia 92, 569 - 575 (2016).

1) Primordial stacking faults?

Defect etch for delineation of stacking faults





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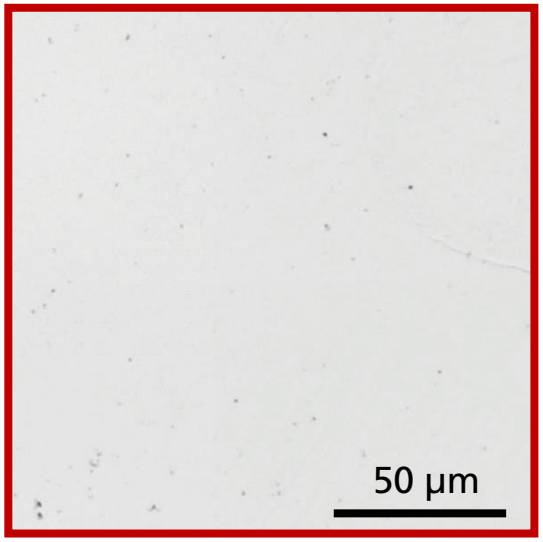
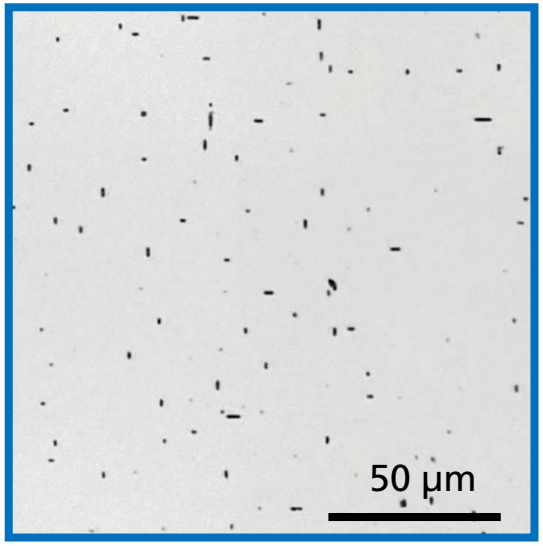
1) Primordial stacking faults?

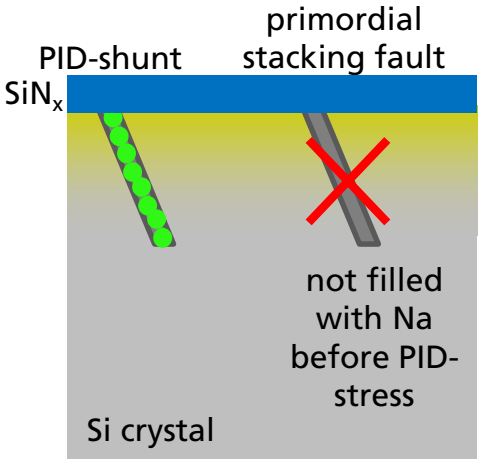
Defect etch for delineation of stacking faults

before PID test



after PID test





- Etch experiment reveals no stacking faults before high voltage stress, too

→ Planar defects (“stacking faults”) don’t exist before high voltage stress

[1] V. Naumann et al., Investigations on the formation of stacking fault-like PID-shunts, Energy Procedia 92, 569 - 575 (2016).

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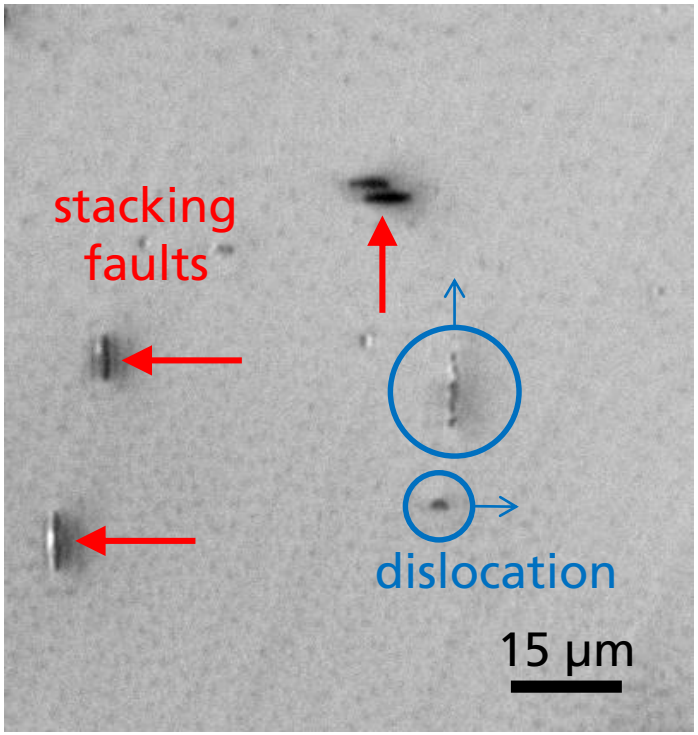
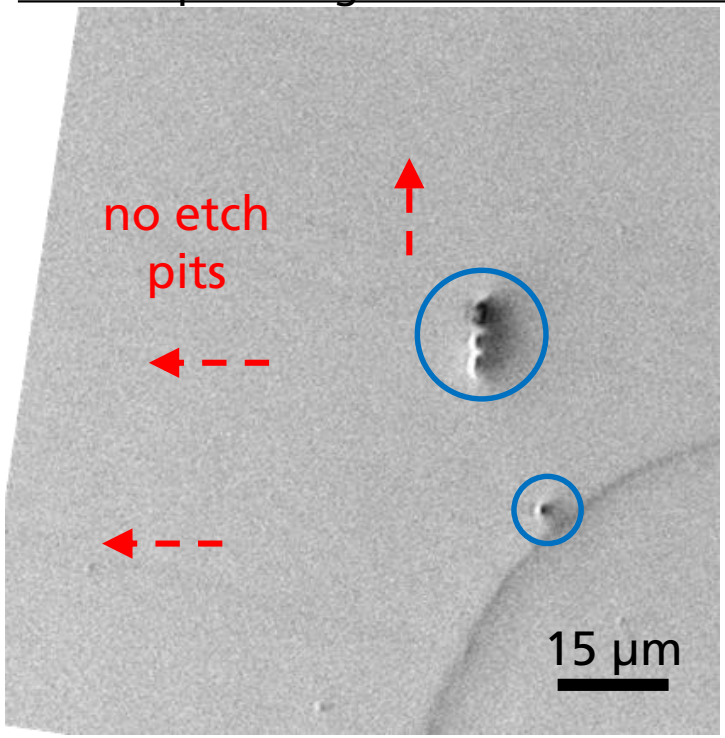
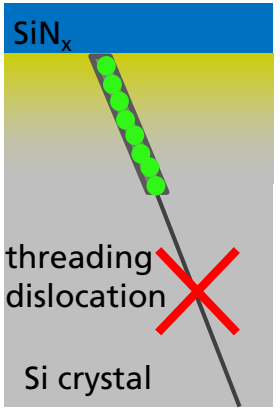
2) Threading dislocations?

Defect etch before and after polish

Removal of SiN + Secco defect etch ➡ Surface polishing + Secco defect etch







- Defect etch before and after ~5…10 µm surface polish

→ Exclusion of threading dislocations as origins for PID-s

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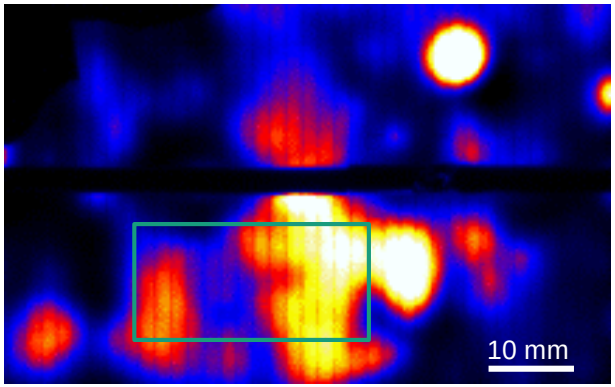
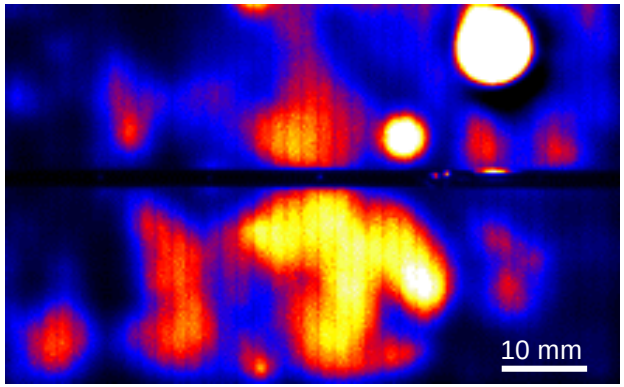
3) Correlation with (micro)structural surface defects?

Comparison of PID-s on neighboring cells – macro scale

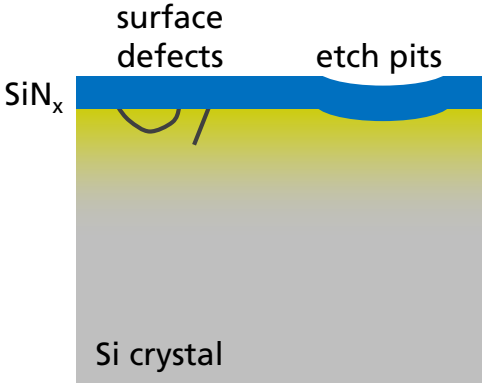
Lock-in thermography in PID stressed area:



cell 1



cell 2



- PID-shunts at same positions on a millimeter scale
- Indication for surface defects initially responsible for evolution of PID-s defects

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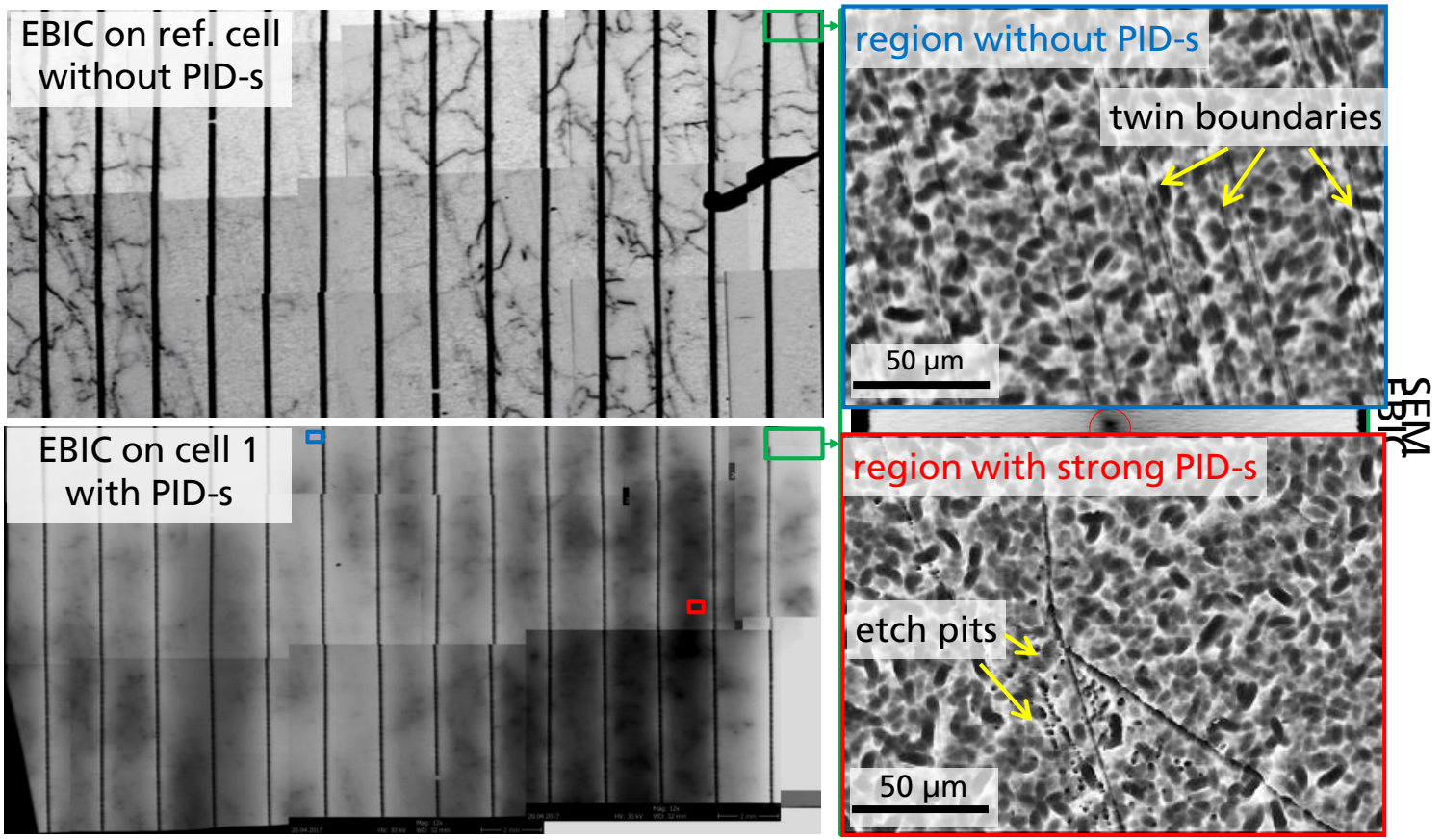
3) Correlation with (micro)structural surface defects?

Comparison of PID-s on neighboring cells – micro scale



- Higher PID-shunt density at recombination active grain boundaries
- Region with strong PID-s shows less twin boundaries and more etch pits

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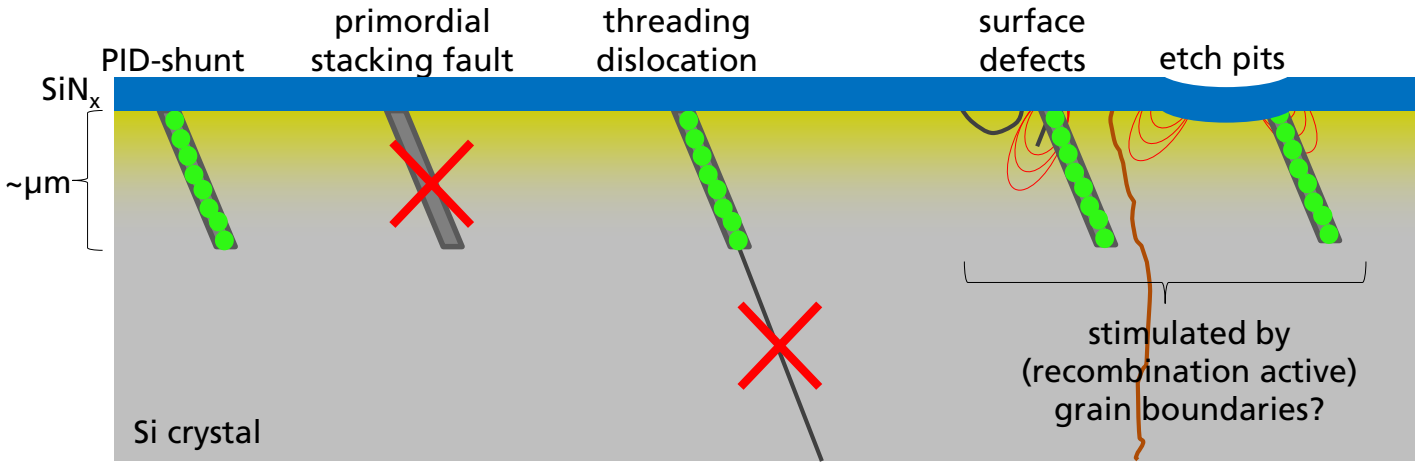
Conclusion

Model for the origin of PID-shunts:

- No primordial stacking faults
- Threading dislocations not at PID-shunt positions
- Origins of PID-shunts seem to be related to surface defects
- High stress at etch pits (enhanced by recombination active GB) or scratches [1]



Stress-related microstructural surface-near defects are points of origin for PID-shunts, i.e. weak points for incorporation of Na, leading to evolution of Na filled planar crystal defects

[1] V. Naumann et al., Investigations on the formation of stacking fault-like PID-shunts, Energy Procedia 92, 569 - 575 (2016).

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Thank you!

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